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A complete simulation system is mapped to a heterogeneous FPGA platform as shown in Figure 2. Presently, we support both Amazon EC2 F1 instances and Xilinx Zynq boards as FPGA-host platforms. 3 STATE SNAPSHOTTING AND INITIALIZATION The Strober framework implements automatic scanchain insertion to

capture RTL state snapshots for sample-based power modeling [13]. The DESSERT framework uses this ...

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